Digital Systems

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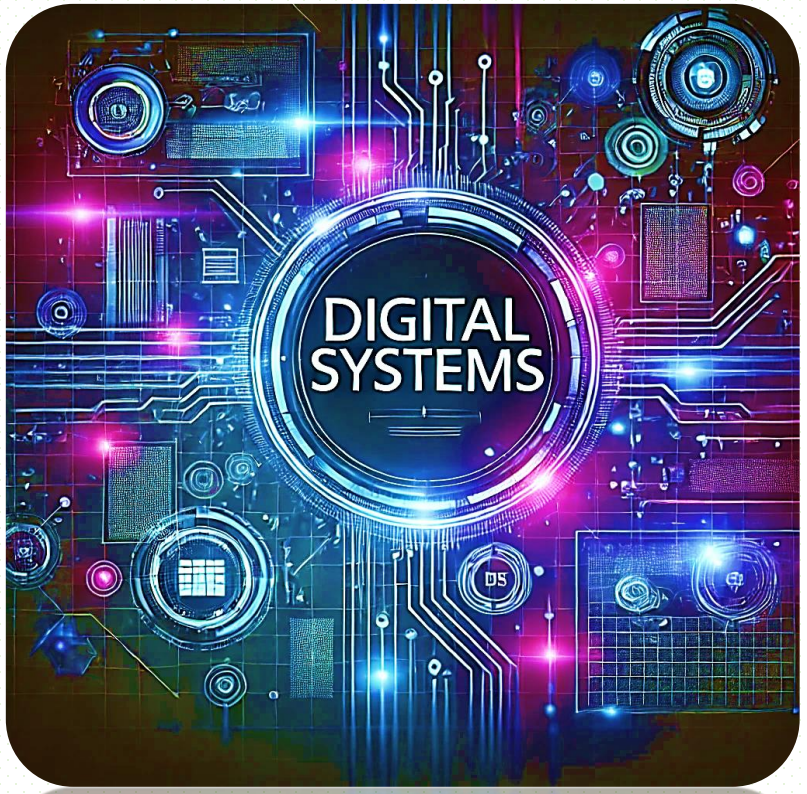
Ashur University



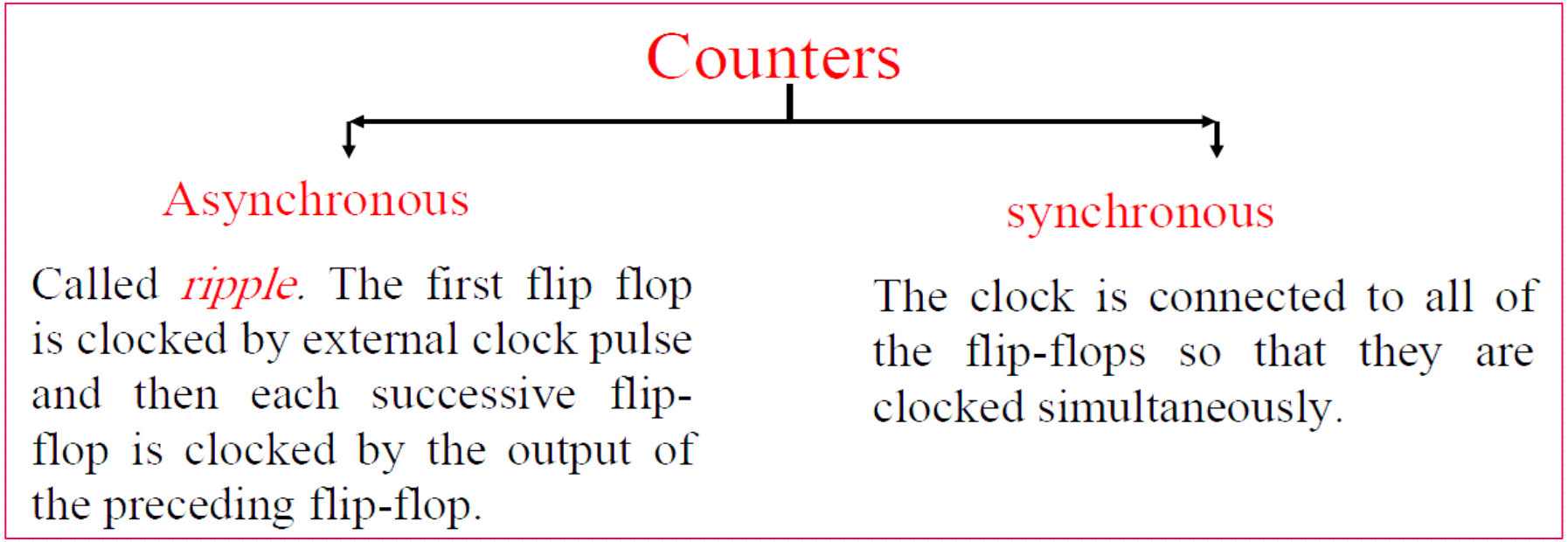
Computer Techniques Engineering Department

Counters

Introduction:

Flip-flops can be connected together to perform counting operations.

Such a group of flip-flops is a counter. The number of flip-flops used and the way in which they are connected determine the number of states Called the Modulus and also the specific sequence of states that the counter goes through during each complete cycle.



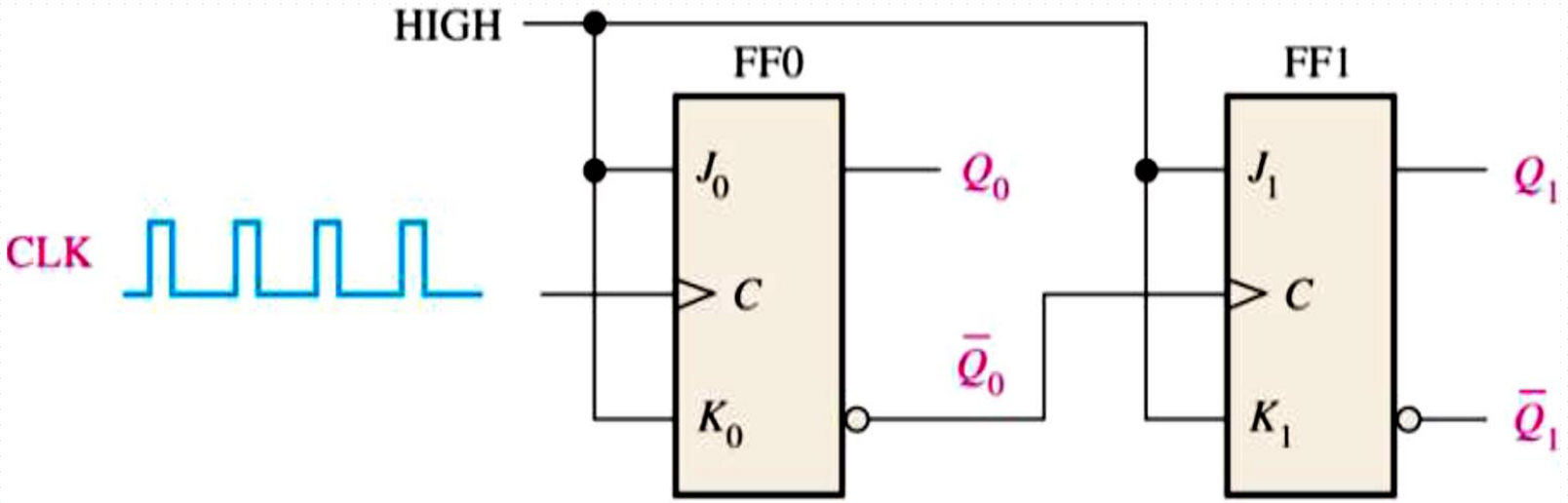
Asynchronous Counters

- **Asynchronous binary counter:**
  - – 2-bit asynchronous binary counter
  - – 3-bit asynchronous binary counter
  - – 4-bit asynchronous binary counter
- **Asynchronous decade counter**

Asynchronous Counters

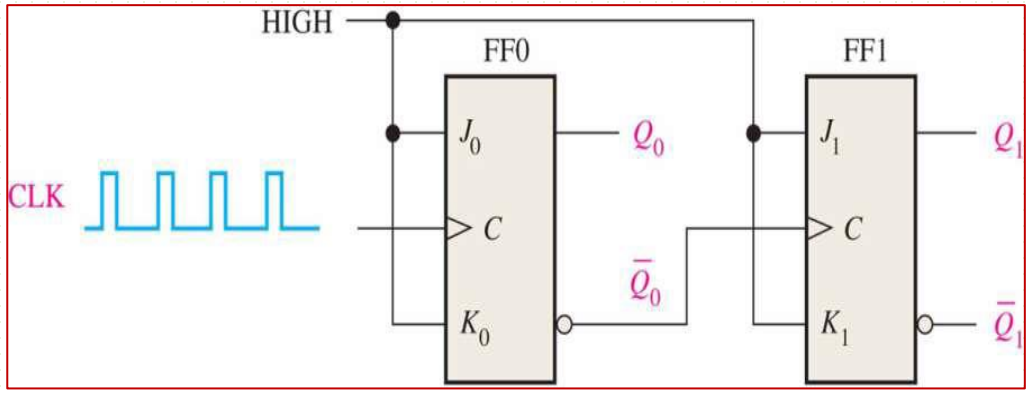
The term asynchronous refers to events that do not have a fixed time relationship with each other and, generally do not occur at the same time. An asynchronous counter is one in which the flip-flops within the counter do not change states at exactly the same time because they do not have a common clock pulse.

Because of the inherent propagation delay time through a flip-flop, a transition of the input clock pulse (CLK) and a transition of the output of FF0 can never occur at exactly the same time. Therefore, the two flip-flops are never simultaneously triggered, so the counter operation is asynchronous



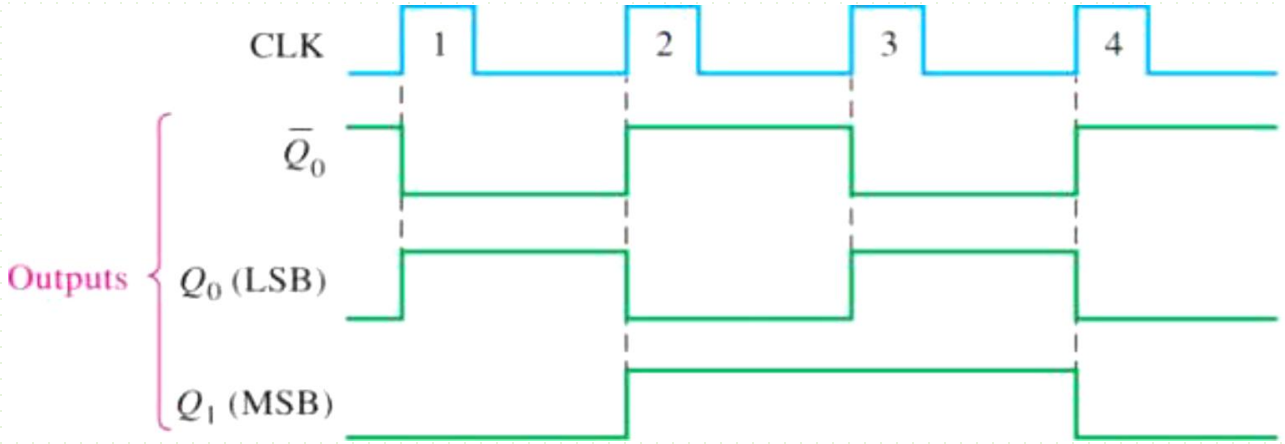
2Bit Asynchronous Binary Counter

J-k Flip Flop



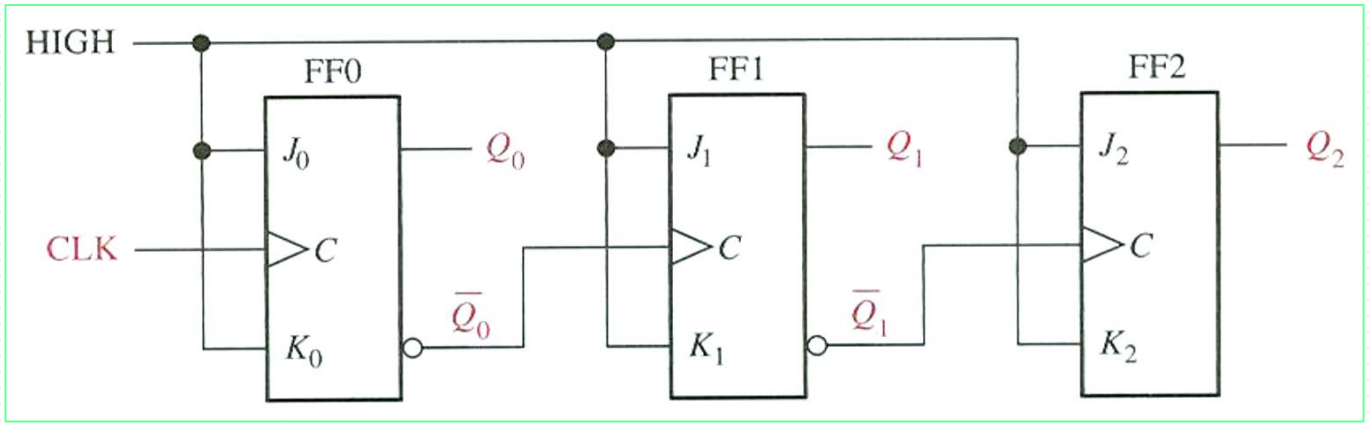
The Timing Diagram :- Both flip-flops are connected for toggle operation (J=1,K=1) and are assumed to be initially RESET (Q LOW)

CLOCK PULSE	Q_1	Q_0
Initially	0	0
1	0	1
2	1	0
3	1	1
4 (recycles)	0	0

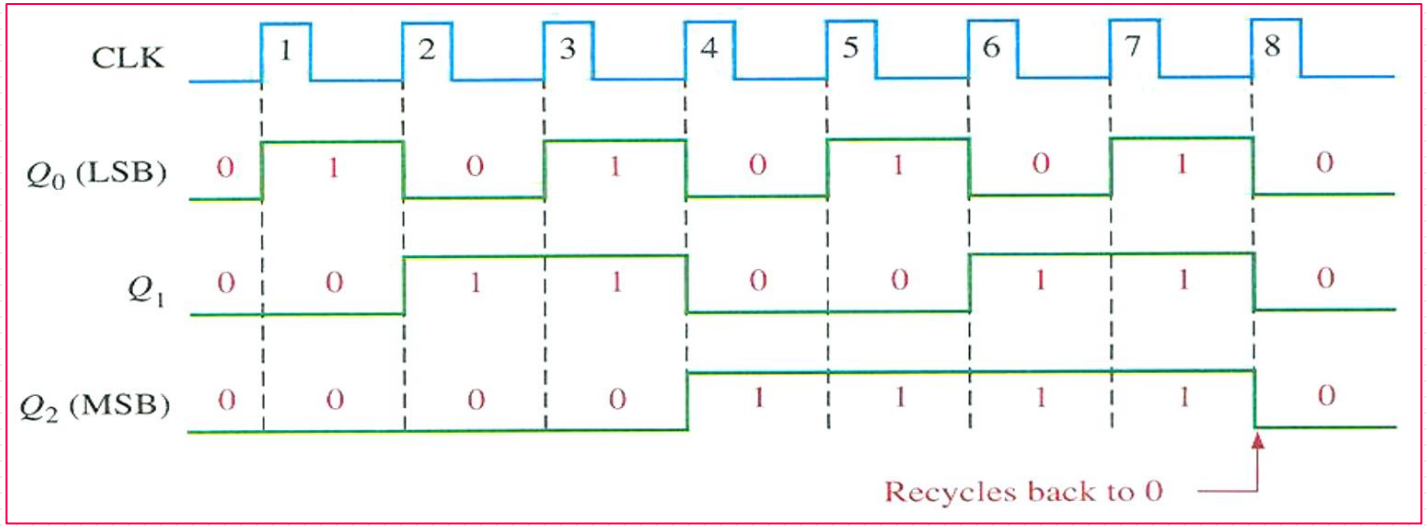


3Bit Asynchronous Binary Counter

J-k Flip Flop



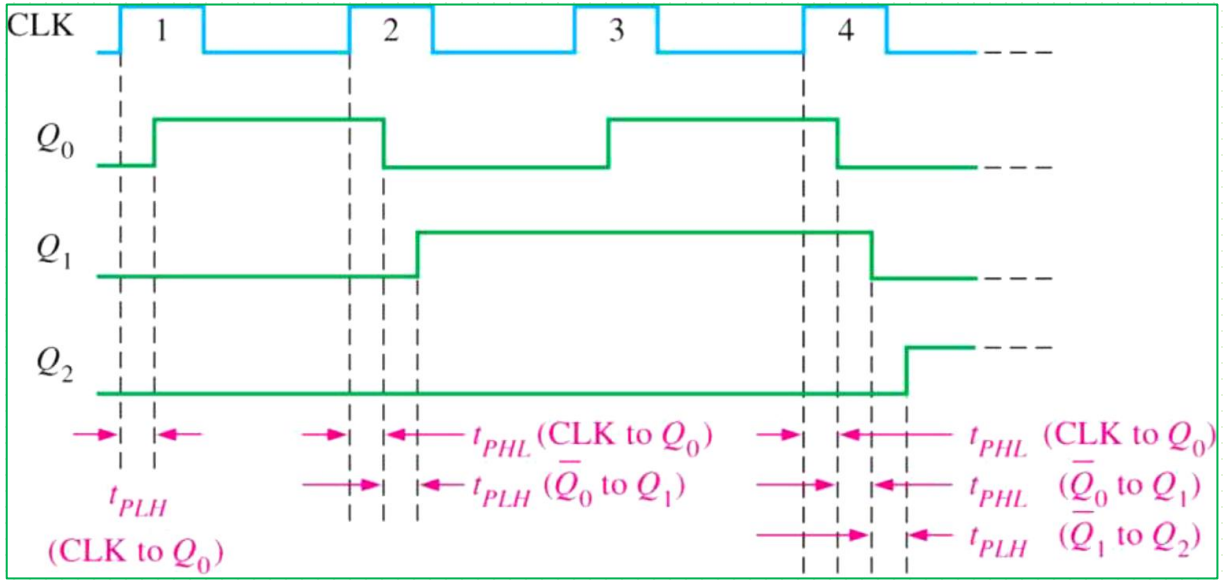
CLOCK PULSE	Q_2	Q_1	Q_0
Initially	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1
8 (recycles)	0	0	0



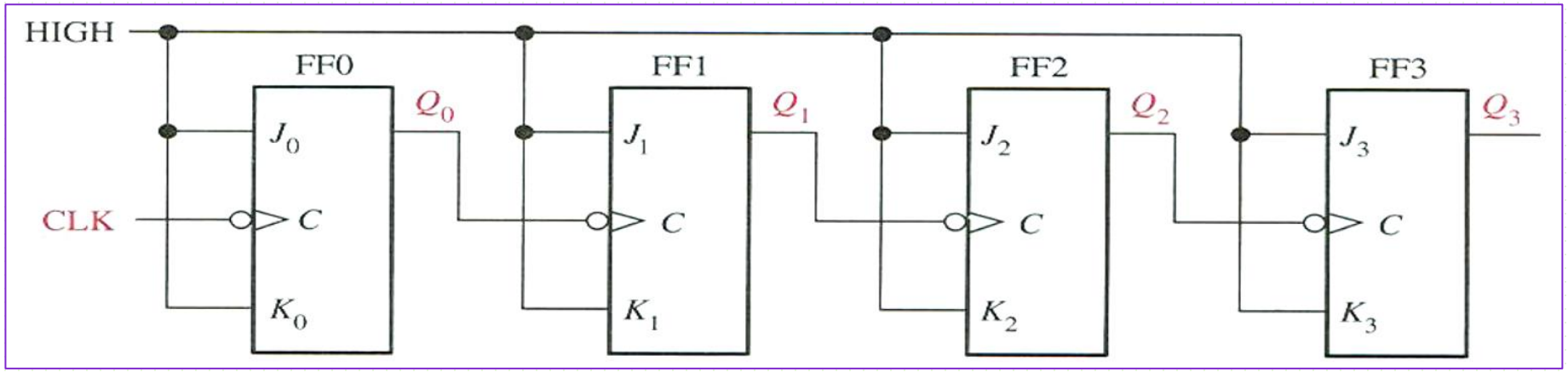
Asynchronous Binary Counter Delay

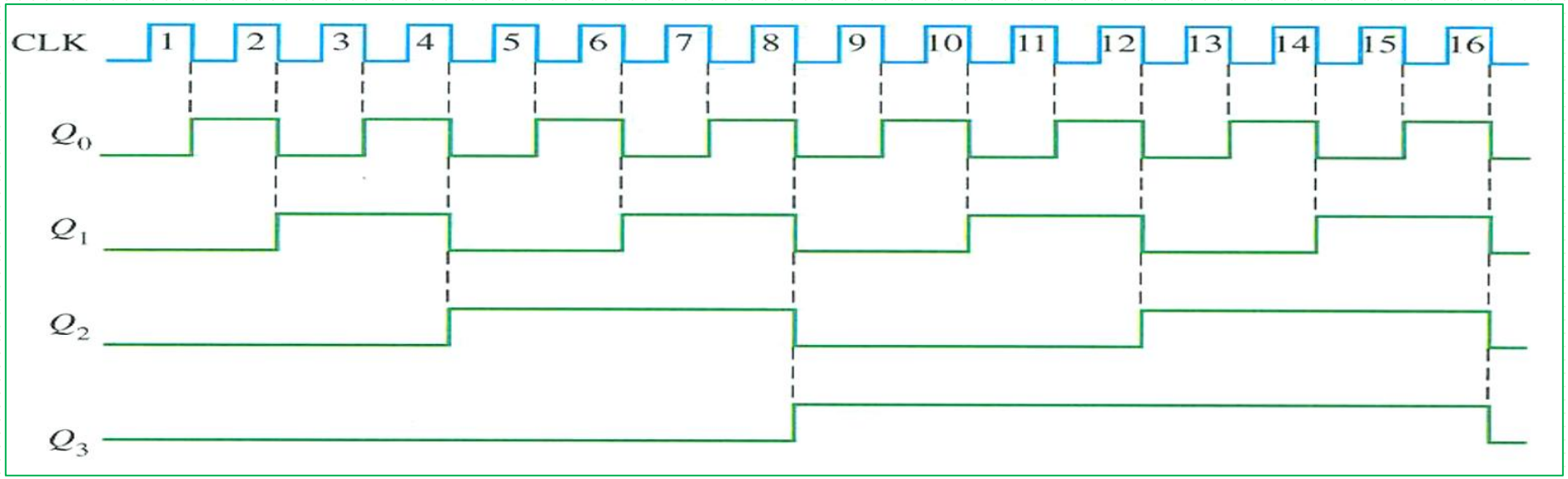
❖ **Propagation Delay:-** Asynchronous counters are commonly referred to as **Ripple counters** for the following reasons:-

- 1. The effect of the input clock pulse is first “felt” by FF0. this effect cannot get to FF1 immediately because of the propagation delay through FF0.
- 2. The propagation delay through FF1 before FF2 can be triggered. Thus the effect of an input clock pulse “ripples” through the counter, taking some time, due to propagation delays, to reach the last flip-flop.



4Bit Asynchronous Binary Counter

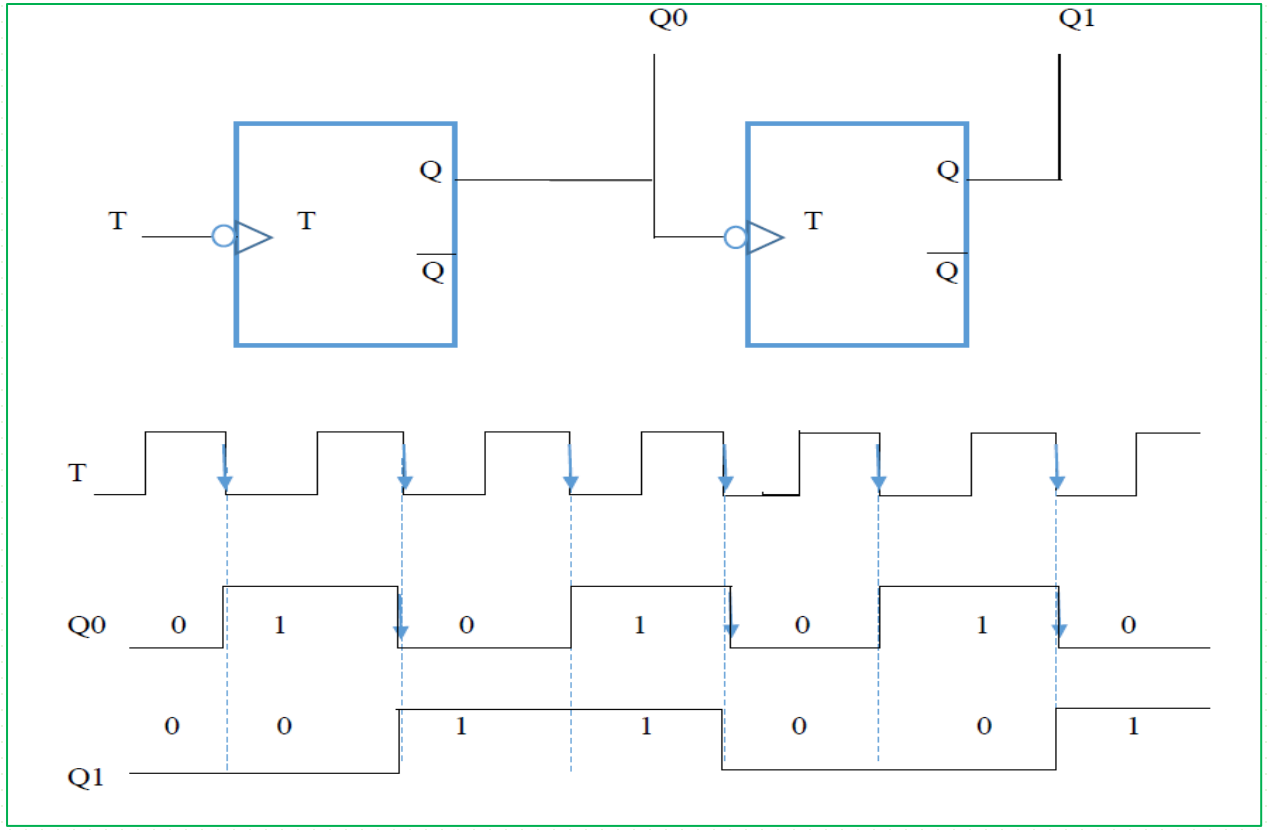




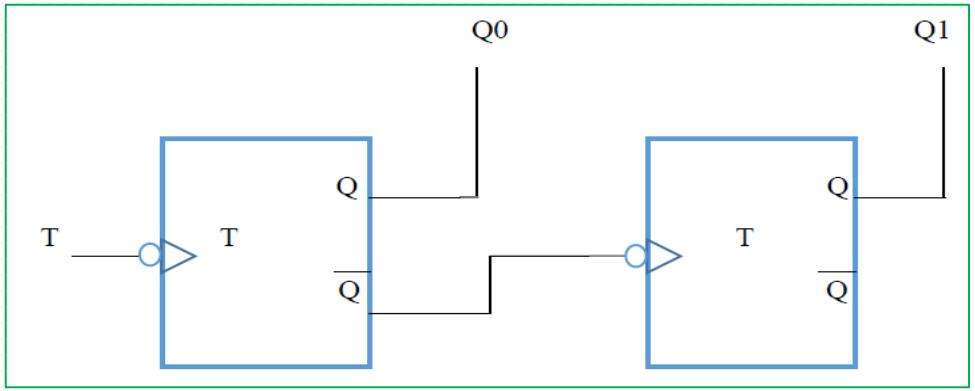
2Bit Asynchronous Binary Counter

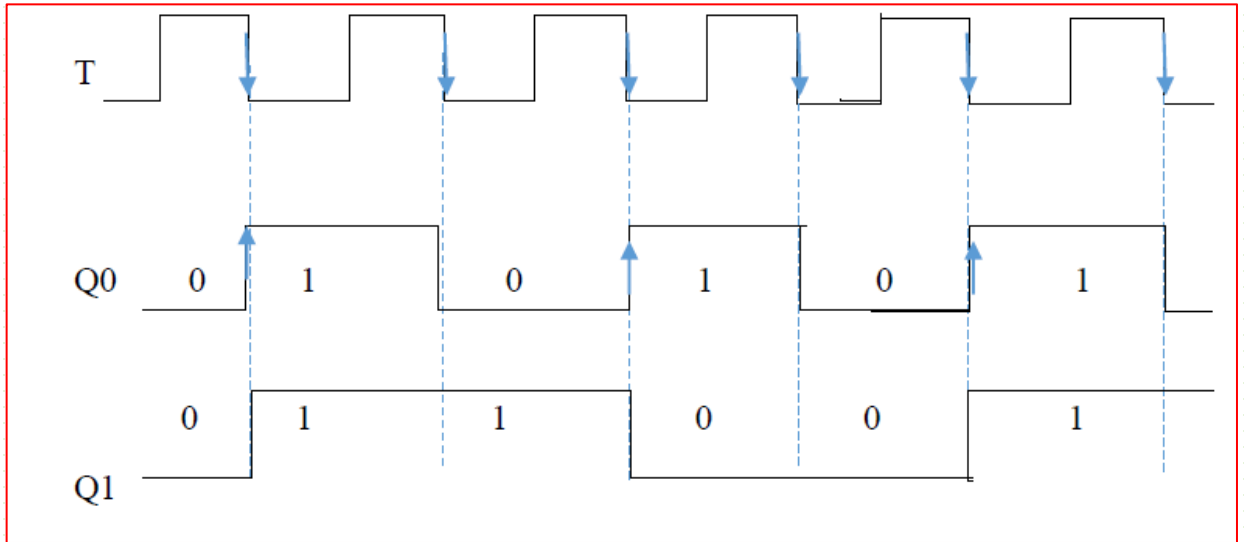
T Flip Flop

2Bit Binary Asynchronous Up Counter



2Bit Binary Asynchronous Down Counter

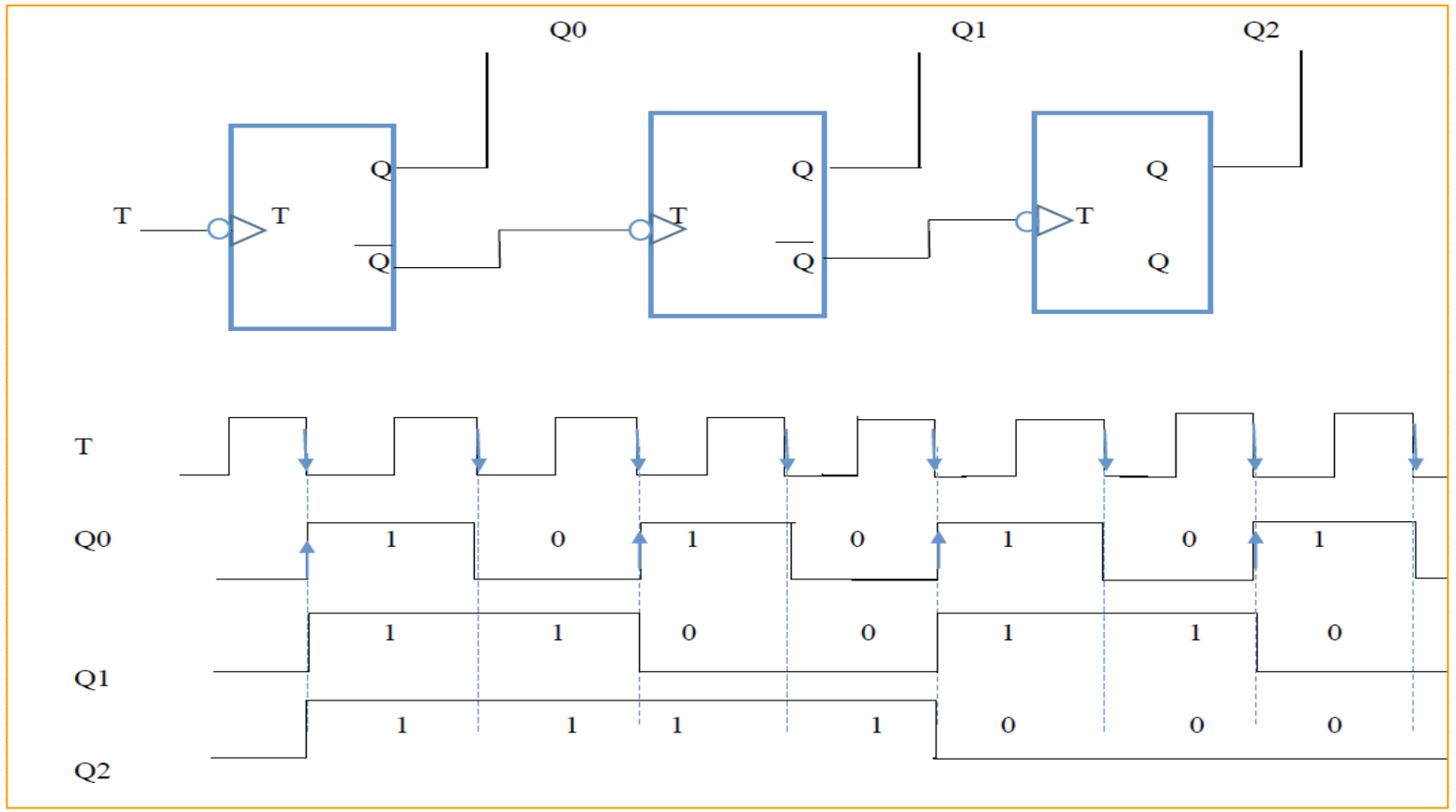




3Bit Asynchronous Binary Counter

T Flip Flop

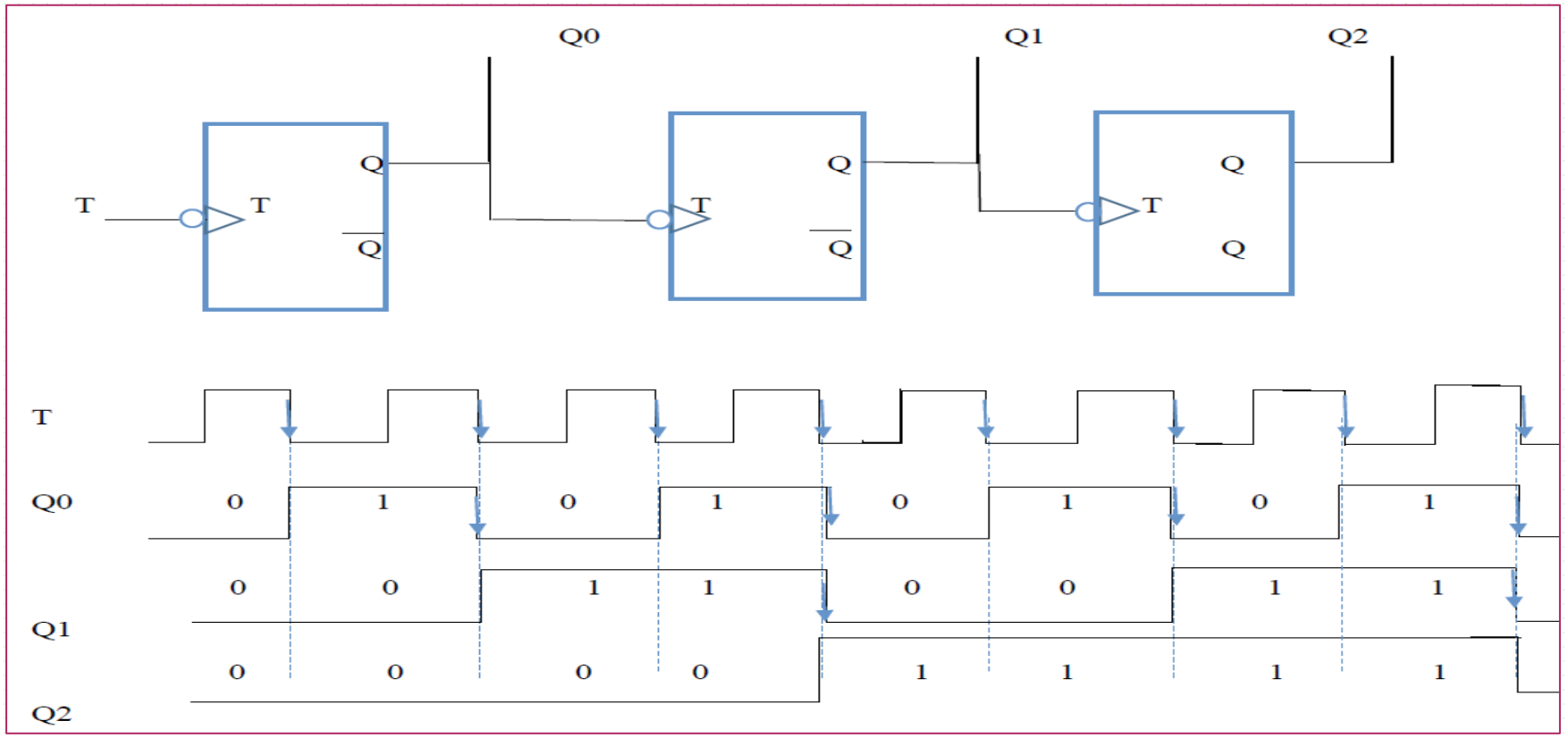
❖ Design 3-bit binary asynchronous down counter and draw timing diagram



2Bit Asynchronous Binary Counter

T Flip Flop

✓ Design 3-bit binary asynchronous up counter and draw timing diagram.



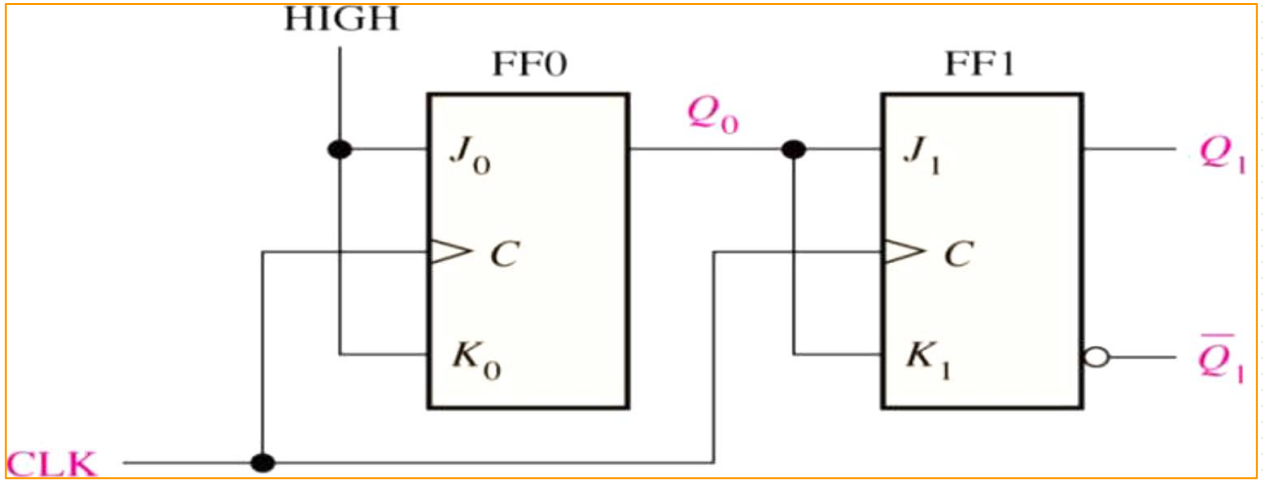
Synchronous Counters

- Synchronous binary counter
  - ✓ 2-bit asynchronous binary counter
  - ✓ 3-bit asynchronous binary counter
  - ✓ 4-bit asynchronous binary counter
- Synchronous decade counter

The term **synchronous** refers to events that have a fixed time relationship with each other. With respect to counter operation, synchronous means that all the flip-flops in the counter are clocked at the same time by a common clock pulse.

2Bit Synchronous Binary Counter

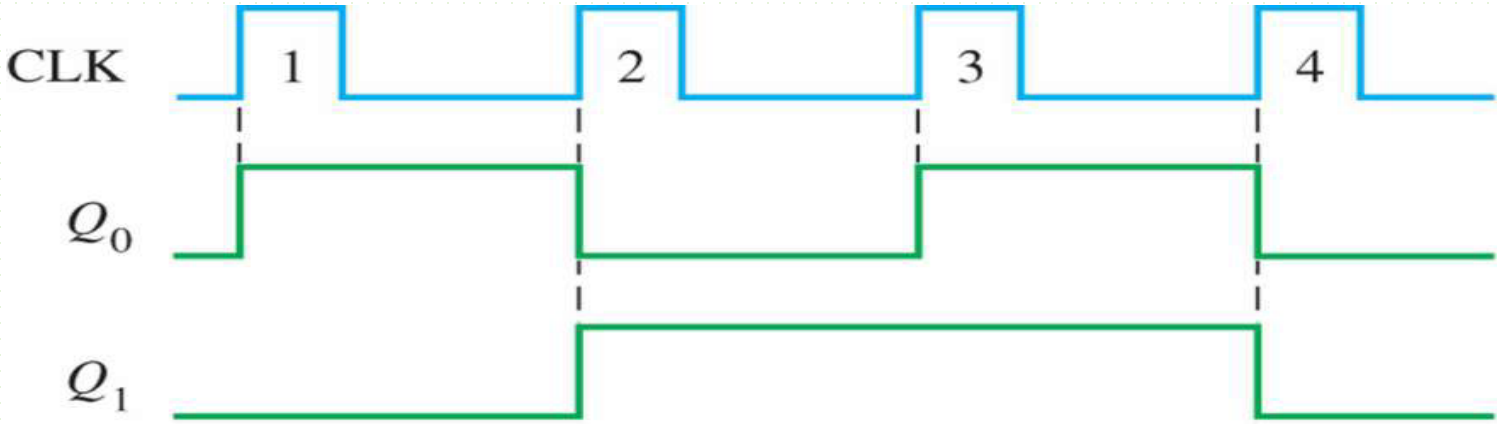
- an arrangement difference from that for the asynchronous counter must be used for the J1 and k1 inputs of FF1 in order to achieve a binary sequence.



2Bit Synchronous Binary Counter

❖The operation of this synchronous counter is as follows:

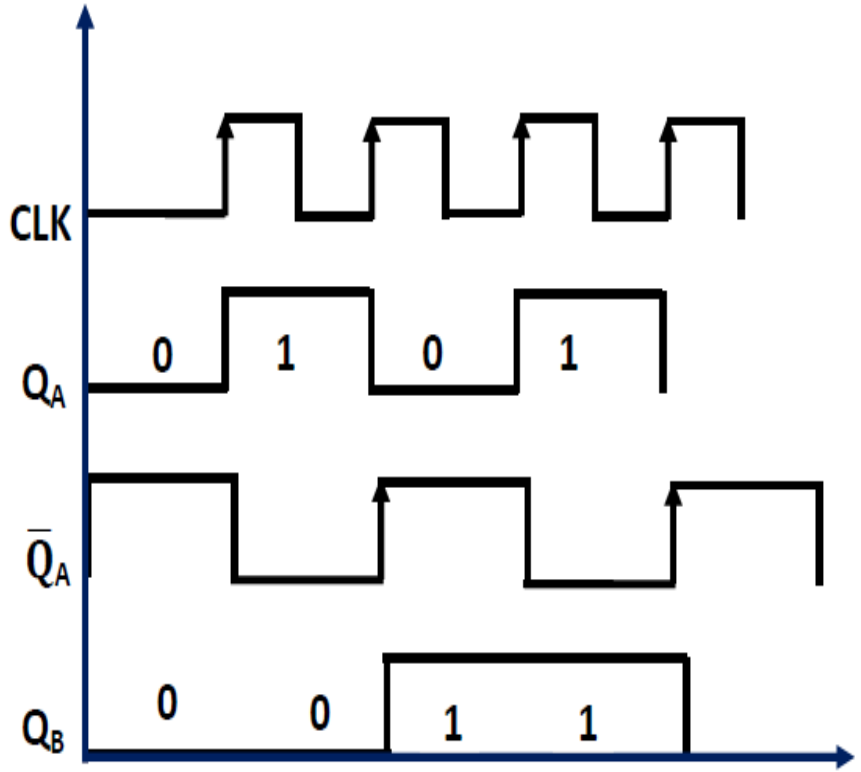
- first, assume that the counter is initially in the binary 0 state; that is, both flip-flops are RESET.
- When the positive edge of the first clock pulse is applied, FF0 will toggle and Q0 will therefore go HIGH.
- Inputs J1 and K1 are both LOW because Q0 to which they are connected, has not yet gone HIGH that mean J=0 and K=0, when the leading edge of the first clock pulse is applied. This is no-change condition, and therefore FF1 does not change state.

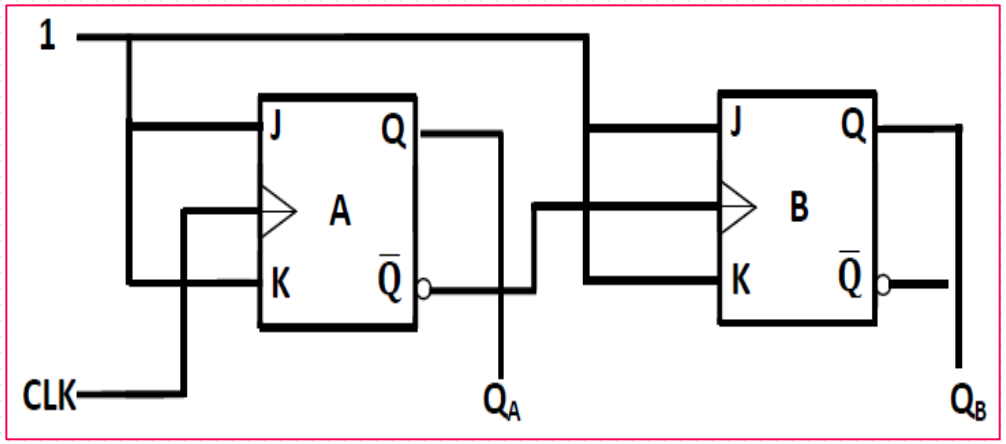


Examples

- design up asynchronous counter has the following sequence (00, 01, 10, and 11) using J-K flip-flops with positive edge clock pulse.
- ✓ draw the timing diagram and truth table.

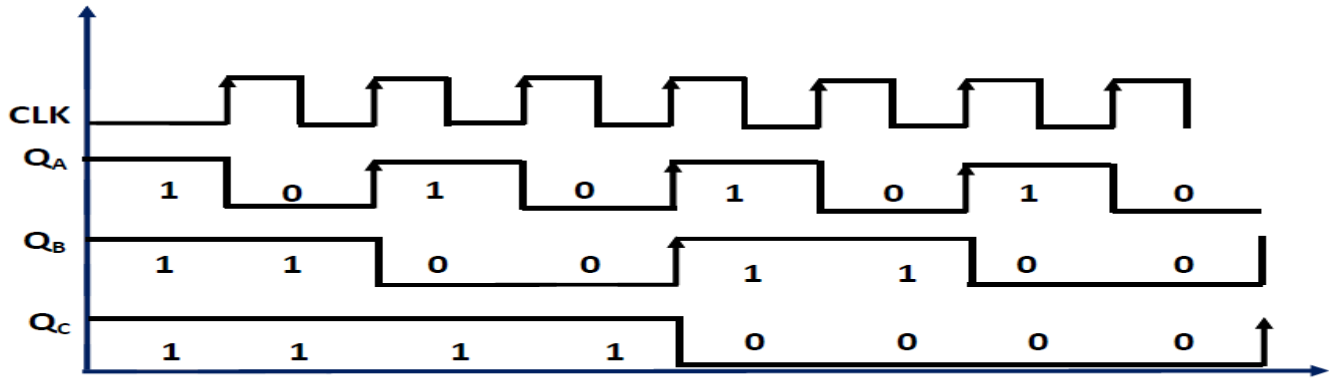
B	A	Output
0	0	0
0	1	1
1	0	2
1	1	3



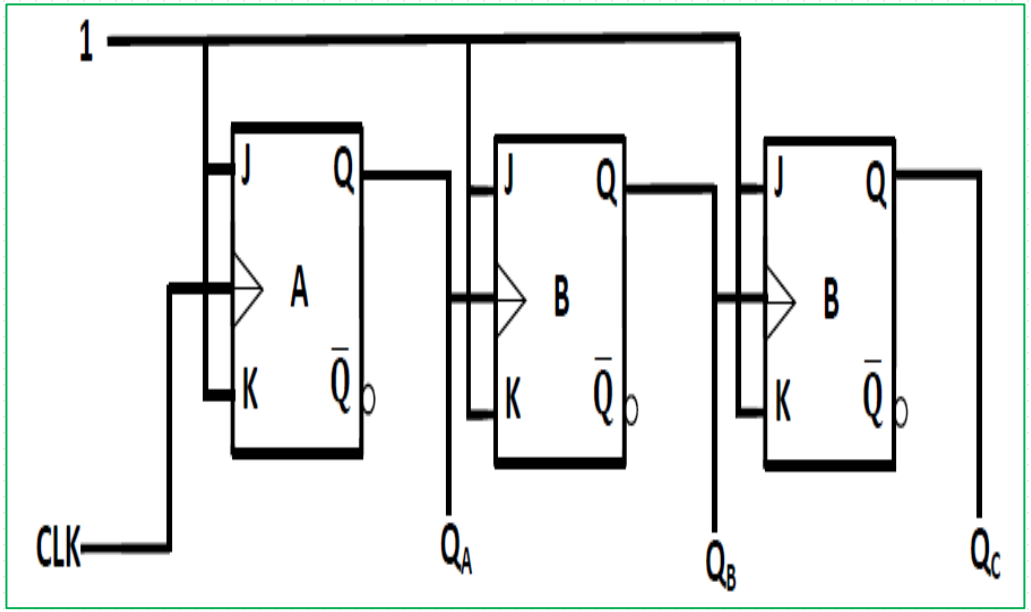


Examples

- design (3-bits) down counter using J-K flip-flops with positive edge clock pulse.
- draw the timing diagram and truth table of the counter



C	B	A	Output
1	1	1	7
1	1	0	6
1	0	1	5
1	0	0	4
0	1	1	3
0	1	0	2
0	0	1	1
0	0	0	0



Examples

- design a (3-bits) down counter using T flip-flops with negative edge clock pulse.
- draw the timing diagram and truth table for this counter.

C	B	A	Output
0	0	0	0
1	1	1	7
1	1	0	6
1	0	1	5
1	0	0	4
0	1	1	3
0	1	0	2
0	0	1	1
0	0	0	0

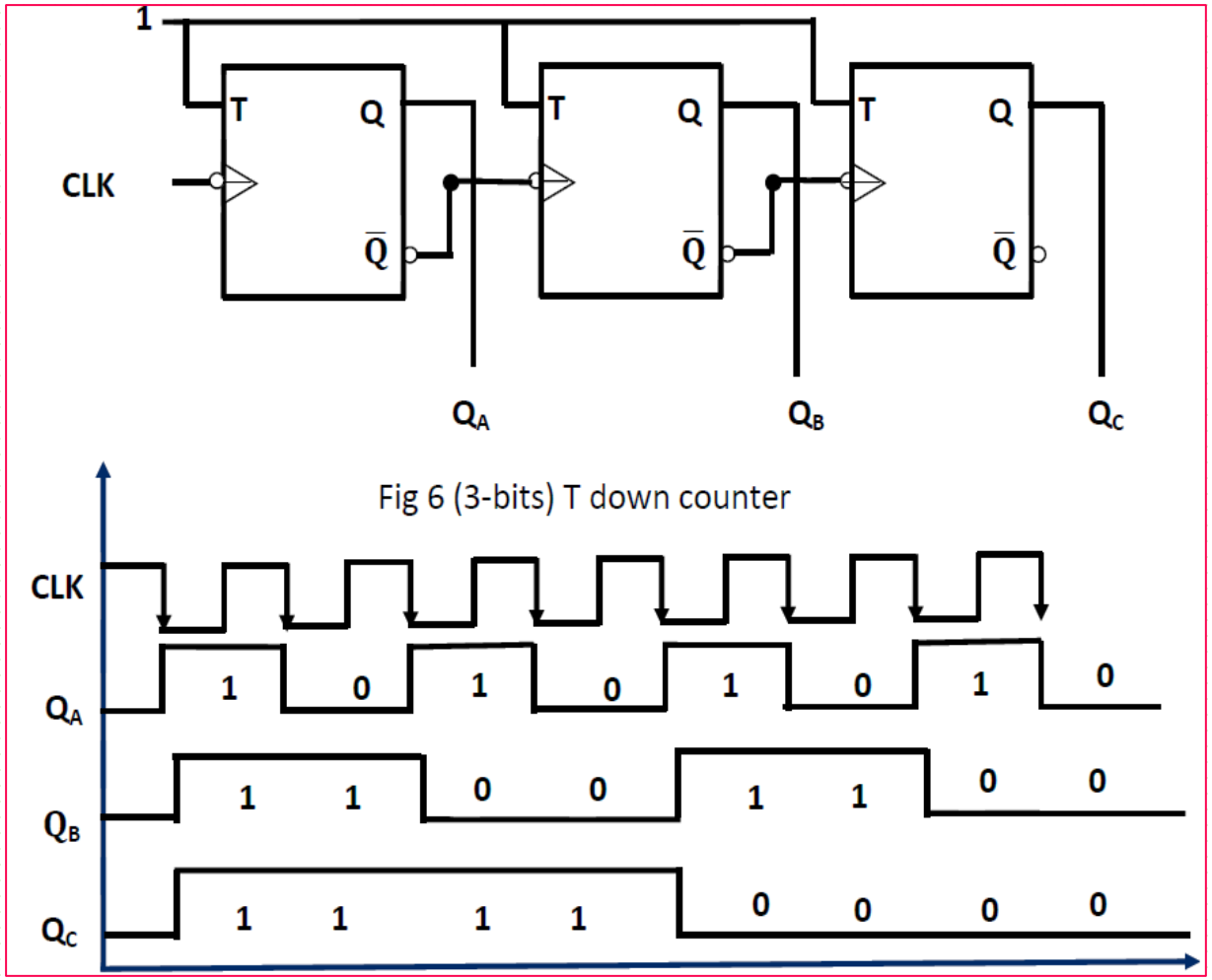


Fig 6 (3-bits) T down counter

Examples

