Digital Systems

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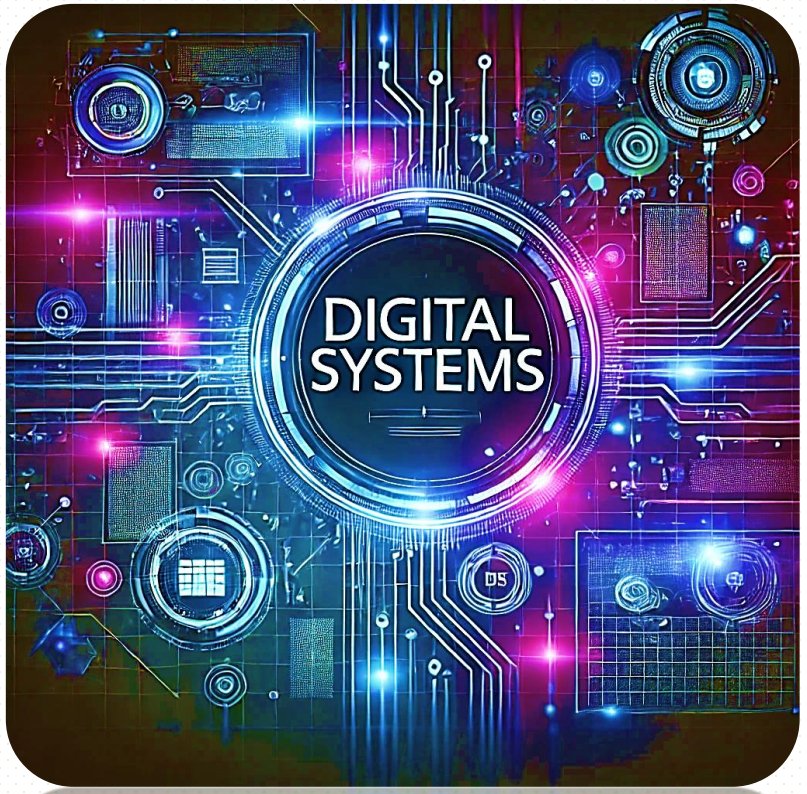
Ashur University



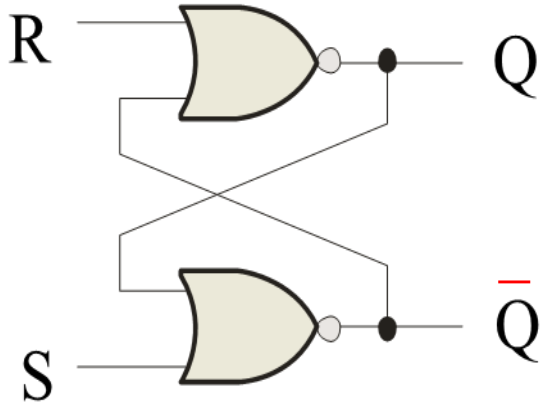
Computer Techniques Engineering Department

Flip-flops

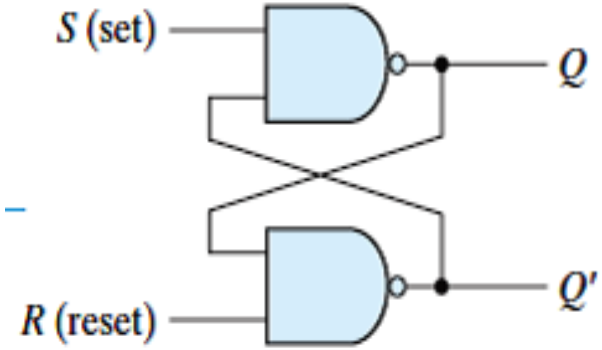
Latches

- A **latch** is a temporary storage device that has two stable states (bistable). It is a basic form of memory.

The **S-R** (Set-Reset) latch is the most basic type. It can be constructed from NOR gates or NAND gates. With NOR gates, the latch responds to active-HIGH inputs; with NAND gates, it responds to active-LOW inputs.



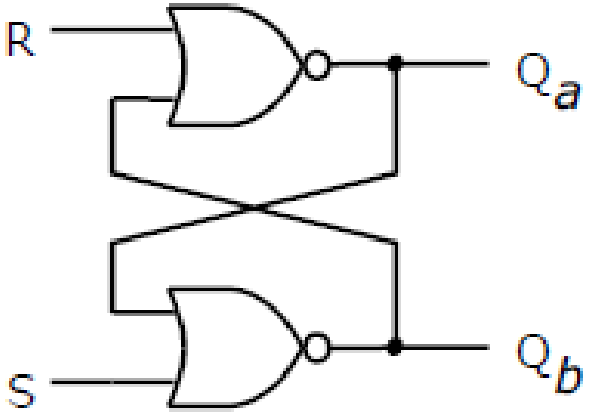
NOR Active-HIGH Latch



NAND Active-LOW Latch

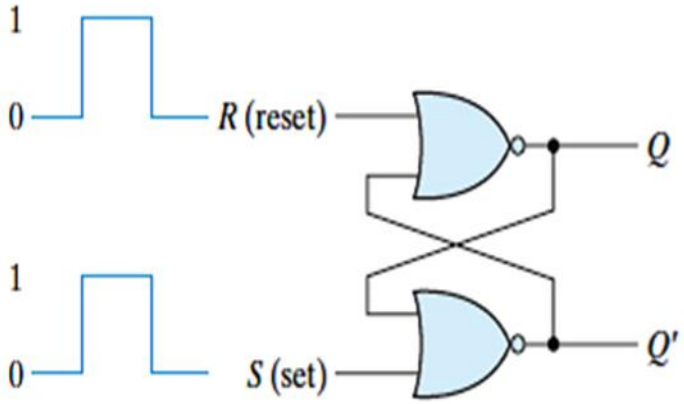
Basic SR latch

- When R=S=0 the circuit remains in its current state (either Q_a=1 and Q_b=0 or Q_a=0 and Q_b=1)
- When S=1 and R=0, the latch is ***set*** into a state where Q_a=1 and Q_b=0
- When S=0 and R=1, the latch is ***reset*** into a state where Q_a=0 and Q_b=1
- Where S=1 and R=1, Q_a=Q_b=0 (there are actually problems with this state as we will see)



S	R	Q_a	Q_b	
0	0	0/1	1/0	(no change)
0	1	0	1	
1	0	1	0	
1	1	0	0	

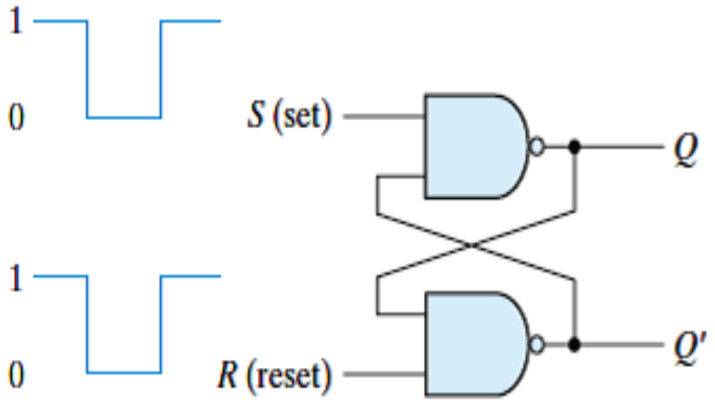
SR Latch



(a) Logic diagram

S	R	Q	Q′	
1	0	1	0	
0	0	1	0	(after $S = 1, R = 0$)
0	1	0	1	
0	0	0	1	(after $S = 0, R = 1$)
1	1	0	0	(forbidden)

(b) Function table



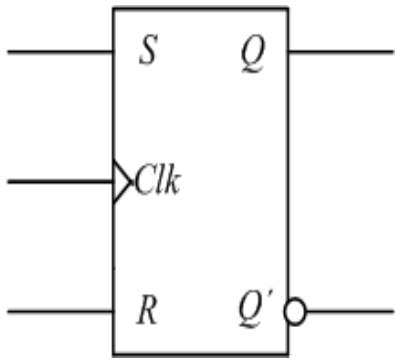
(a) Logic diagram

S	R	Q	Q′	
1	0	0	1	
1	1	0	1	(after $S = 1, R = 0$)
0	1	1	0	
1	1	1	0	(after $S = 0, R = 1$)
0	0	1	1	(forbidden)

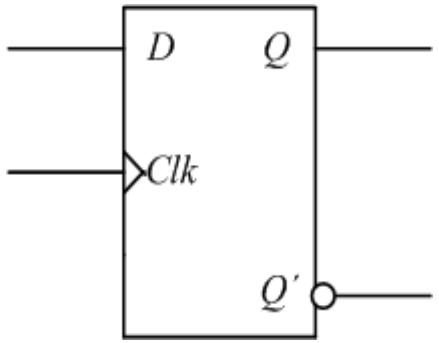
(b) Function table

Flip-flops

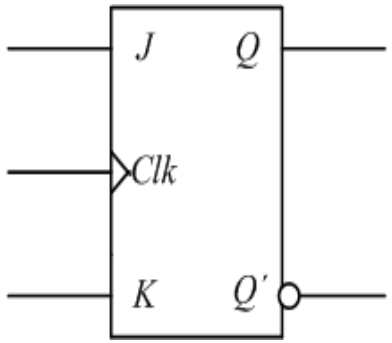
- A device that stores either a 0 or 1.
- Stored value can be changed only at certain times determined by a clock input.
- New value depend on the current state and it's control inputs
- A digital circuit that contains flip-flops is called a sequential circuit



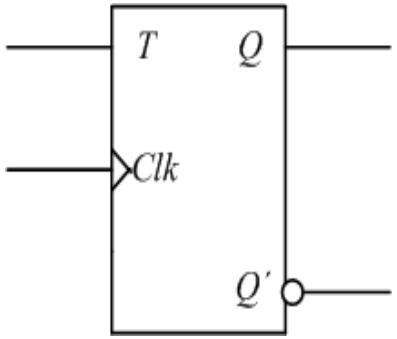
S-R flip-flops



D flip-flop



J-K flip-flops



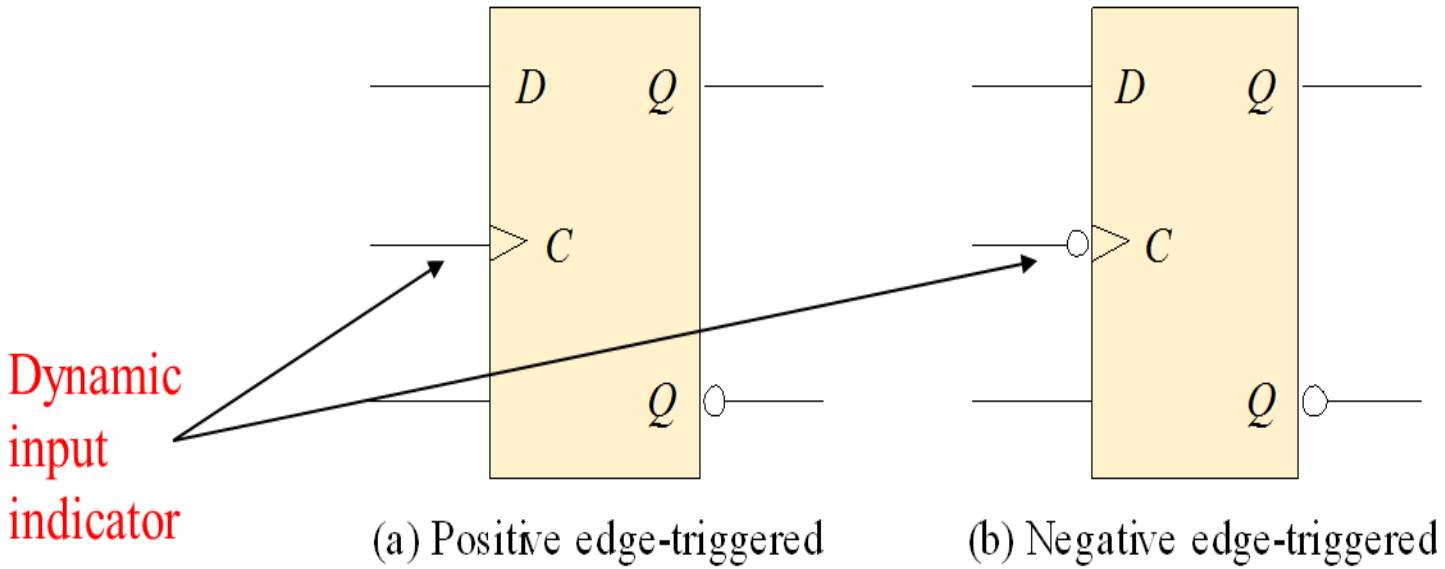
T flip-flop

Flip-flops

Flip-flop :is a clocked device, in which only the clock edge determines when a new bit is entered.

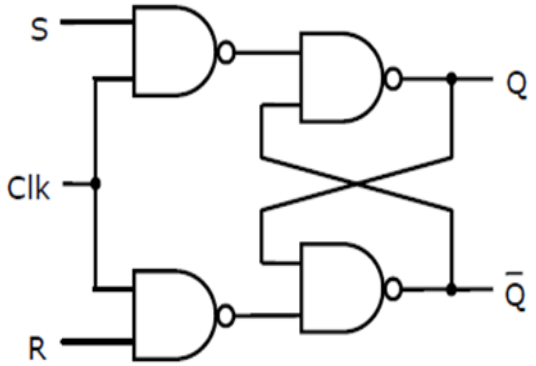
Flip-flop differs from a latch in the manner it changes states.

The active edge can be positive or negative.

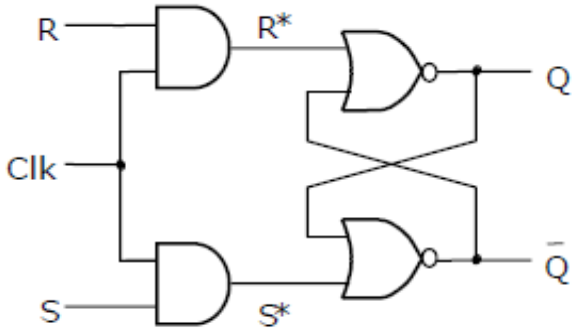


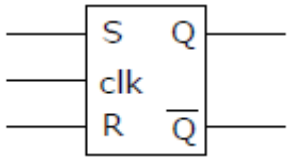
(a) Positive edge-triggered (b) Negative edge-triggered

Gated SR latch timing diagram



OR



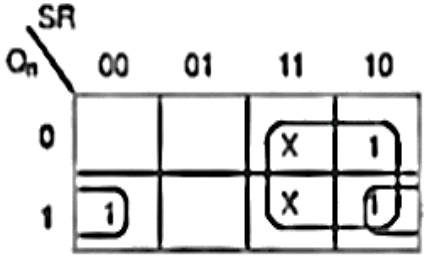


CLK	S	R	Q(t+1)
0	X	X	Q(t)
1	0	0	Q(t)
1	0	1	0
1	1	0	1
1	1	1	X

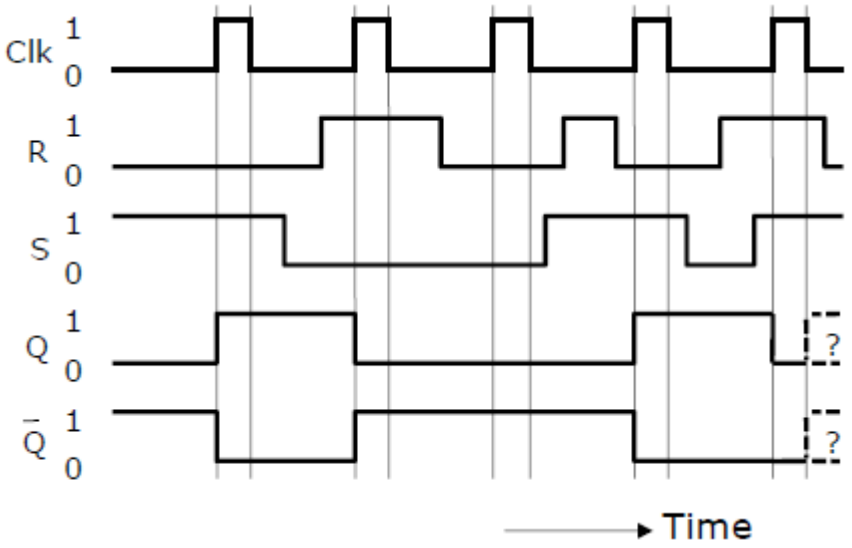
Q(t)=present state
Q(t+1)=next state

Qn	S	R	Q_{n+1}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	Indeter
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	Indeter

Note. Indeter = not used



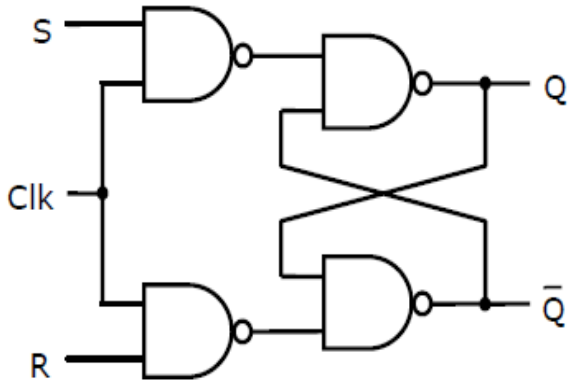
$$Q_{n+1} = S + \bar{R}.Q_n$$



Latches

A gated latch is a variation on the basic latch.

The **gated latch** has an additional input, called enable (*Clk*) that must be HIGH in order for the latch to respond to the *S* and *R* inputs.

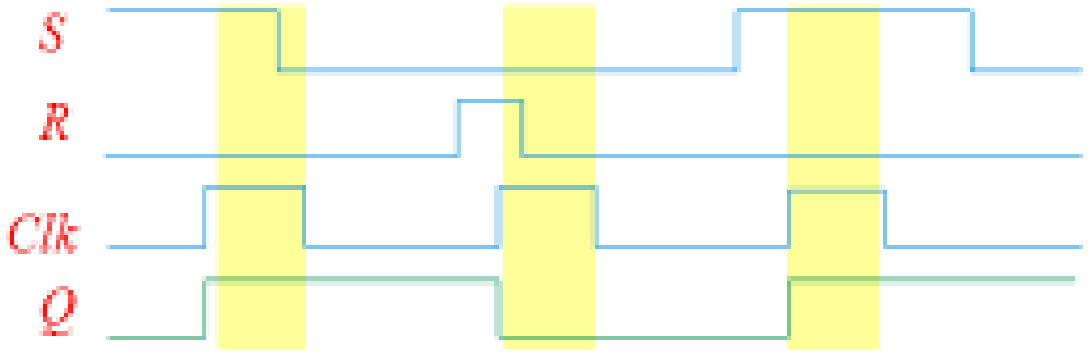


Example:

Show the *Q* output with relation to the input signals. Assume *Q* starts LOW.

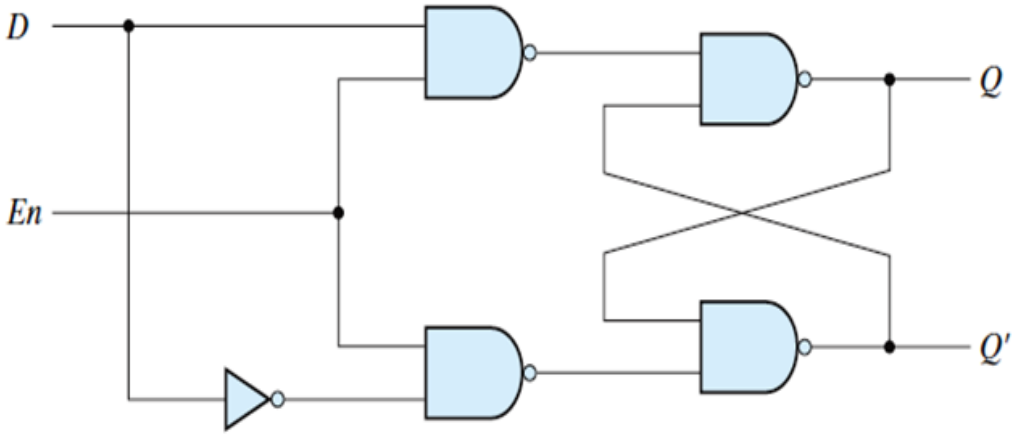
Solution:

Keep in mind that *S* and *R* are only active when *Clk* is HIGH.



D Latches

The *D* latch is an variation of the *S-R* latch but combines the *S* and *R* inputs into a single *D* input as shown:

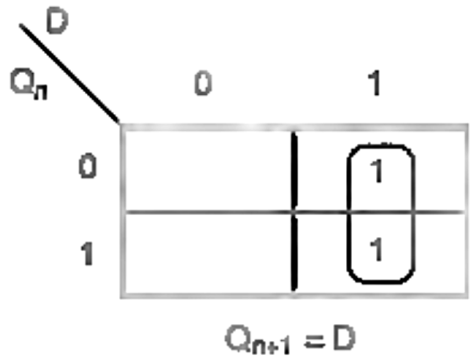


(a) Logic diagram

En	*D*	Next state of *Q*
0	X	No change
1	0	$Q = 0$; reset state
1	1	$Q = 1$; set state

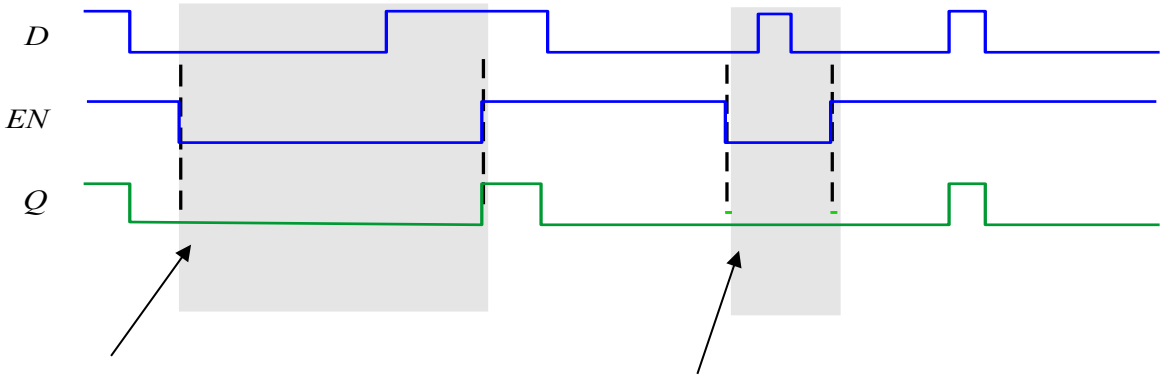
(b) Function table

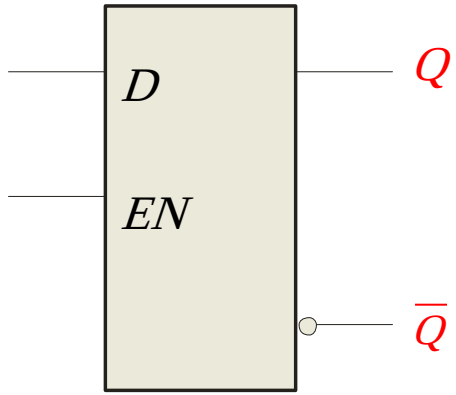
Q_n	D	Q_{n+1}
0	0	0
0	1	1
1	0	0
1	1	1



A simple rule for the *D* latch is: *Q* follows *D* when the Enable is active.

Example

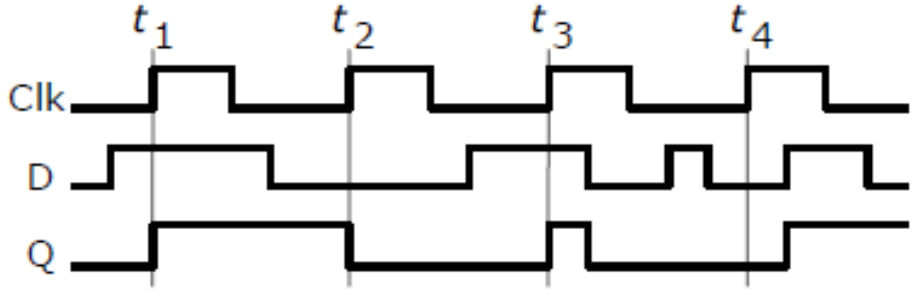




Notice that the Enable is not active during these times, so the output is latched.

The truth table for the *D* latch summarizes its operation. If *EN* is LOW, then there is no change in the output and it is latched.

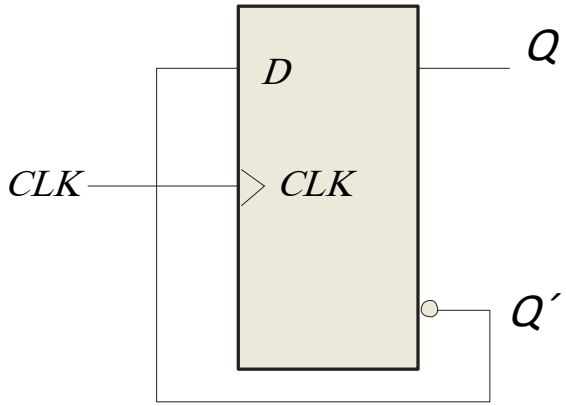
Inputs		Outputs		
D	*EN*	*Q*	$\overline{Q}$	Comments
0	1	0	1	RESET
1	1	1	0	SET
X	0	Q_0	$\overline{Q}_0$	No change



Flip-flops

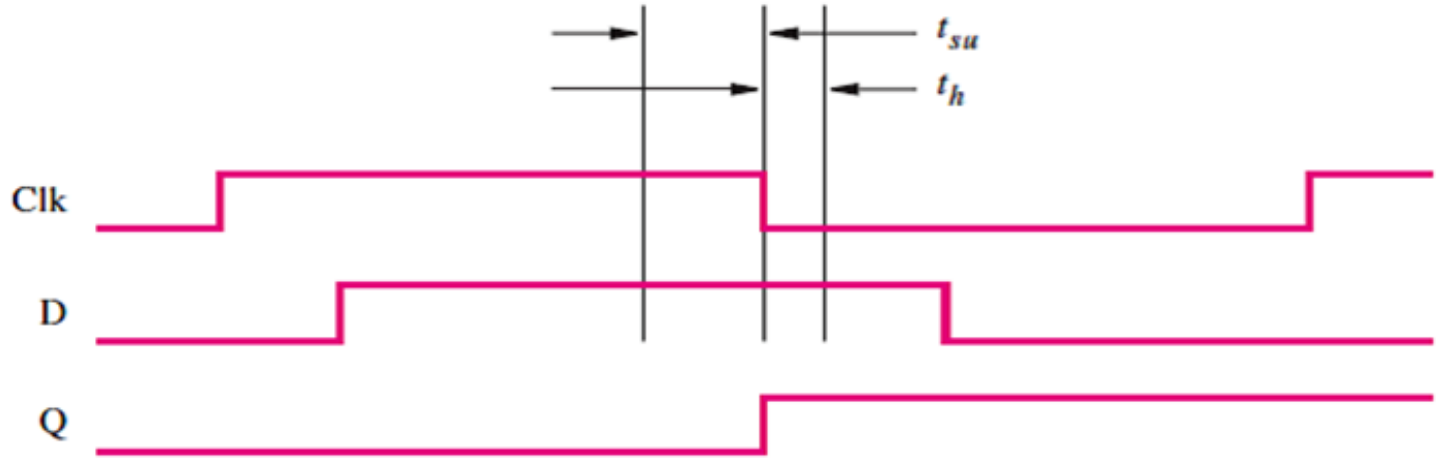
A D-flip-flop does not have a toggle mode like the J-K flip-flop, but you can hardwire a **toggle** mode by connecting $\overline{Q}$ back to D as shown. This is useful in some counters.

For example, if Q is LOW, Q' is HIGH and the flip-flop will toggle on the next clock edge. Because the flip-flop only changes on the active edge, the output will only change once for each clock pulse.



D flip-flop hardwired for a toggle mode

Effects of Propagation Delays



The minimum time that the D signal must be stable prior to the negative edge of the Clk signal is called the **setup time**, t_{su}, of the latch. The minimum time that the D signal must remain stable after the negative edge of the *Clk* signal is called the **hold time, t_h**, of the latch. The values of t_{su} and t_h depend on the technology used. Manufacturers of integrated circuit chips provide this information on the data sheets that describe their chips. Typical values for CMOS technology are t_{su} = 3 ns and t_h = 2 ns.

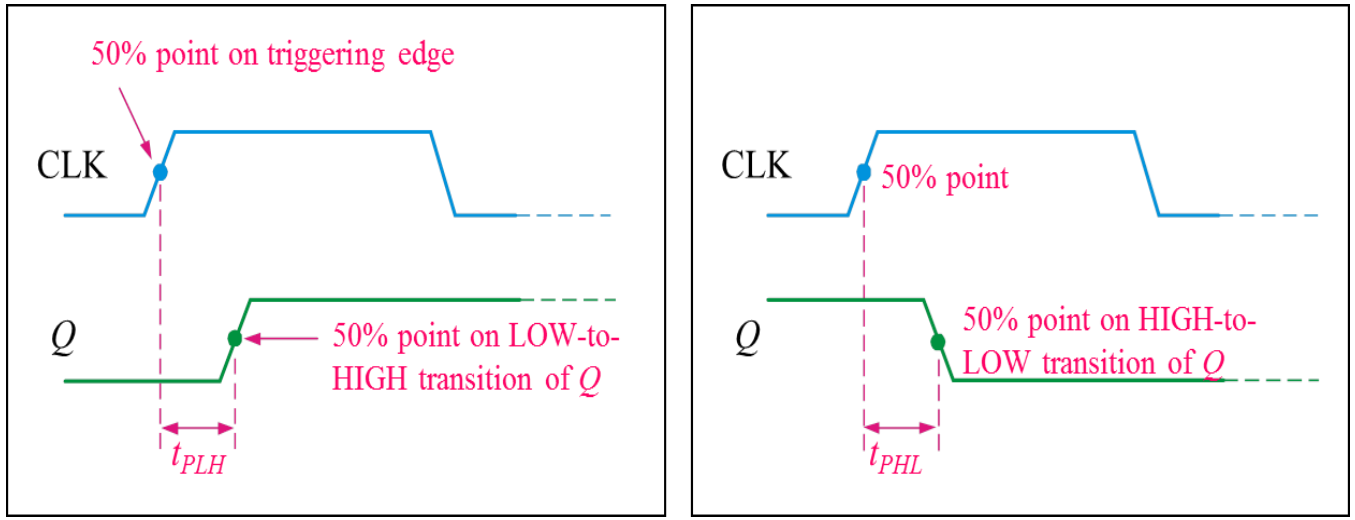
Flip-flop Characteristics

A **flip-flop** is a storage element based on the gated latch principle, which can have its output state changed only on the edge of the controlling clock signal. We considered two types:

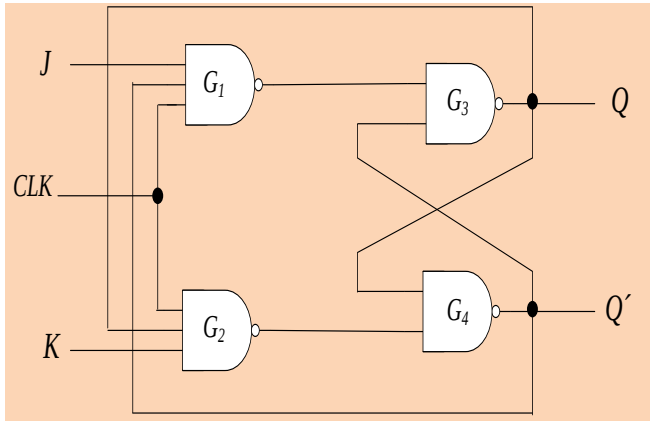
- **Edge-triggered flip-flop** is affected only by the input values present when the active edge of the clock occurs.

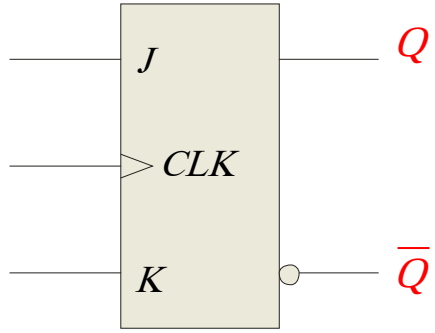
- **Master-slave flip-flop** is built with two gated latches. The master stage is active during half of the clock cycle, and the slave stage is active during the other half.

Propagation delay time is specified for the rising and falling outputs. It is measured between the 50% level of the clock to the 50% level of the output transition



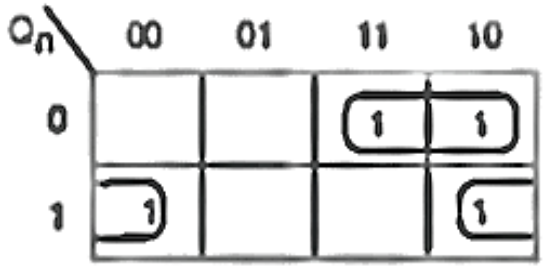
J-K flip-flop





Inputs			Outputs		
J	K	CLK	Q	$\bar{Q}$	Comments
0	0	↑	Q_0	$\bar{Q}_0$	No change
0	1	↑	0	1	RESET
1	0	↑	1	0	SET
1	1	↑	$\bar{Q}_0$	Q_0	Toggle

Q_n	J	K	Q_{n+1}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0



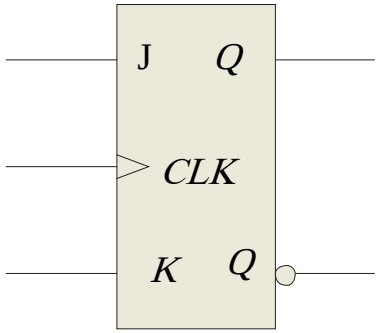
$$Q_{n+1} = J.\bar{Q}_n + \bar{K}.Q_n$$

The J-K flip-flop is more versatile than the D flip flop. In addition to the clock input, it has two inputs, labeled *J* and *K*. When both *J* and *K* = 1, the output changes states (toggles) on the active clock edge (in this case, the rising edge).

Flip-flops

Example

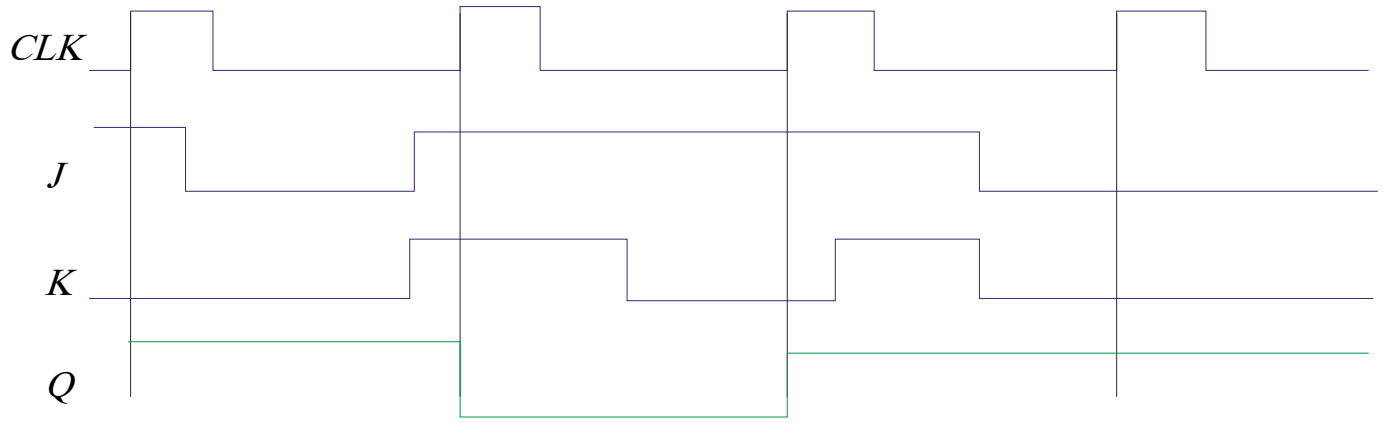
Determine the Q output for the J-K flip-flop, given the inputs shown.



Inputs			Outputs		
J	K	CLK	Q	$\overline{Q}$	Comments
0	0	↑	Q_0	$\overline{Q}_0$	No change
0	1	↑	0	1	RESET
1	0	↑	1	0	SET
1	1	↑	$\overline{Q}_0$	Q_0	Toggle

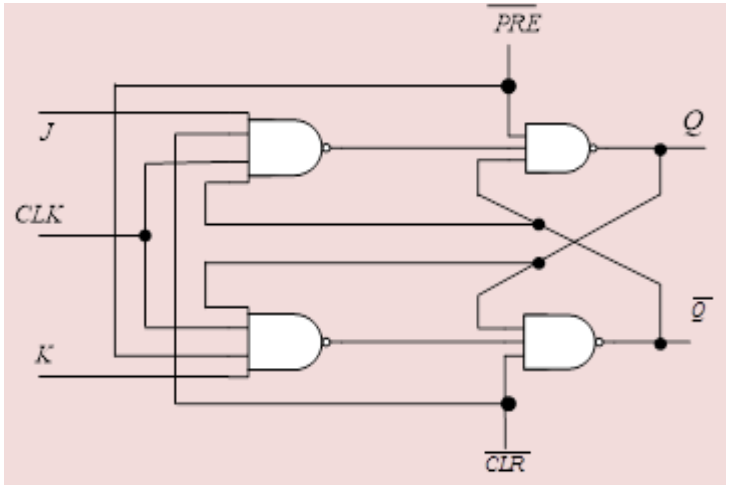
Solution

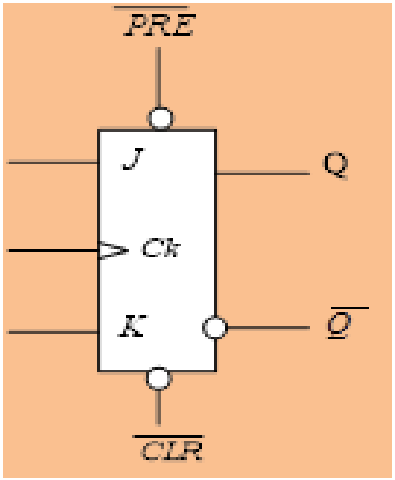
Notice that the outputs change on the leading edge of the clock.



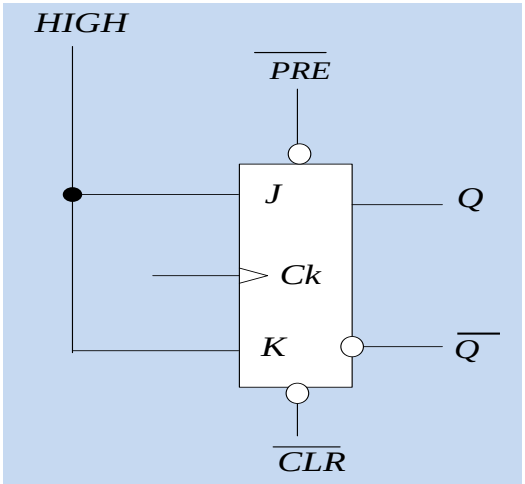
Asynchronous Preset and Clear Inputs Flip-flop

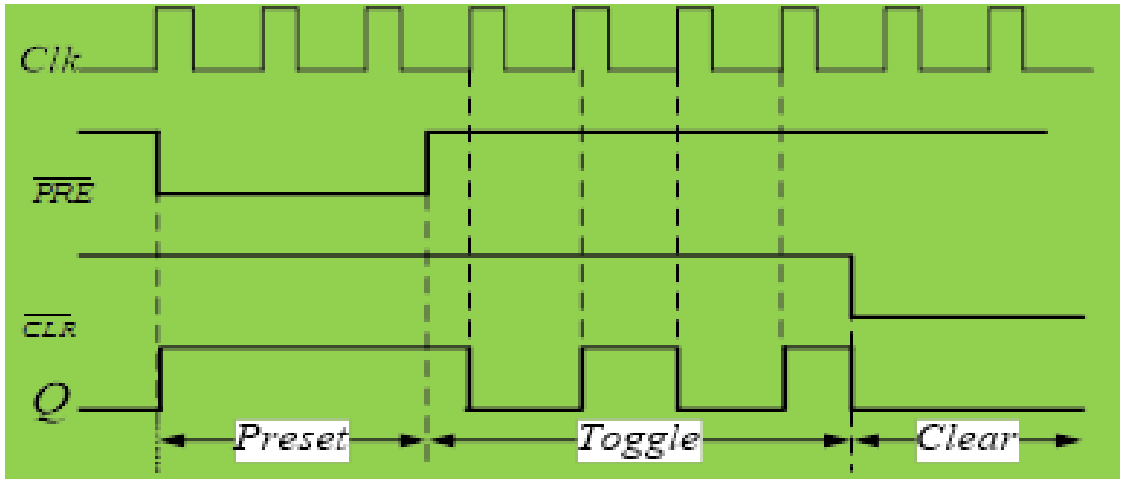
Asynchronous, meaning they affect the output independent of the clock. Two such inputs are normally labeled preset (PRE) and clear (CLR). These inputs are usually active LOW. A J-K flip flop with active LOW preset and CLR is shown





Example



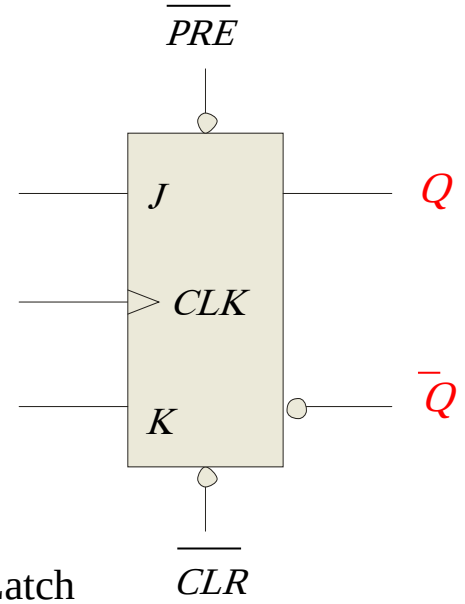


Flip-flops

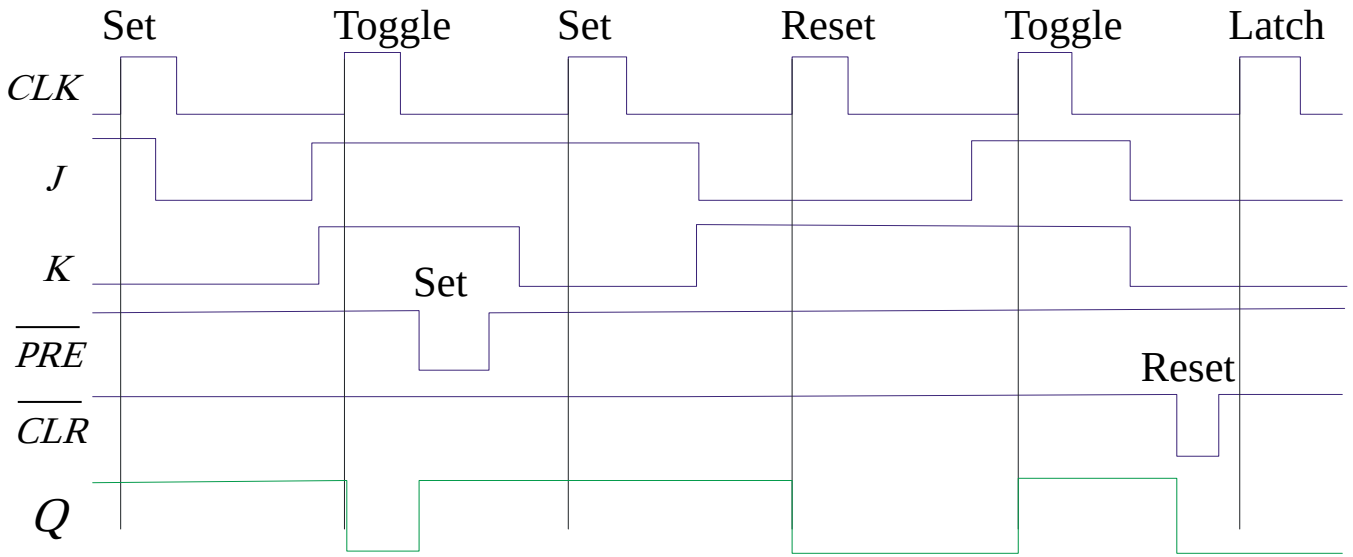
Example

Determine the Q output for the J-K flip-flop, given the inputs shown.

J	K	Q(t+1)
0	0	Q(t)
0	1	0
1	0	1
1	1	Q′(t)



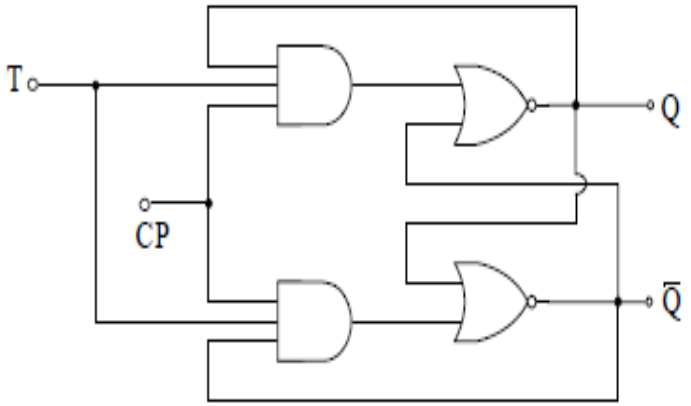
Solution



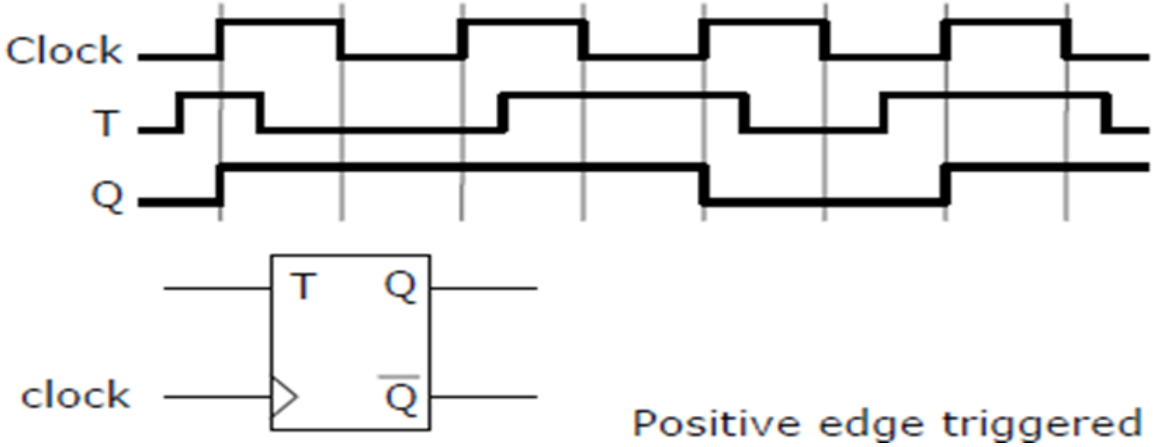
T Flip-flops

The name T derives from the behavior of the circuit, which 'toggles' its state when T=1

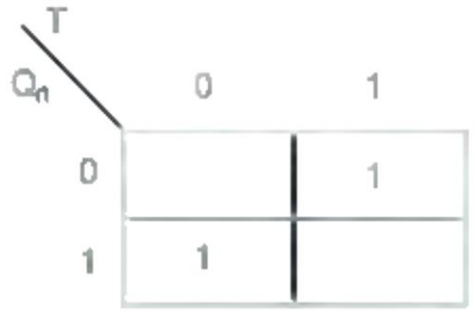
- This feature makes the T flip-flop a useful element when constructing counter circuits



Input	Present State	Next State
T	Q_n	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

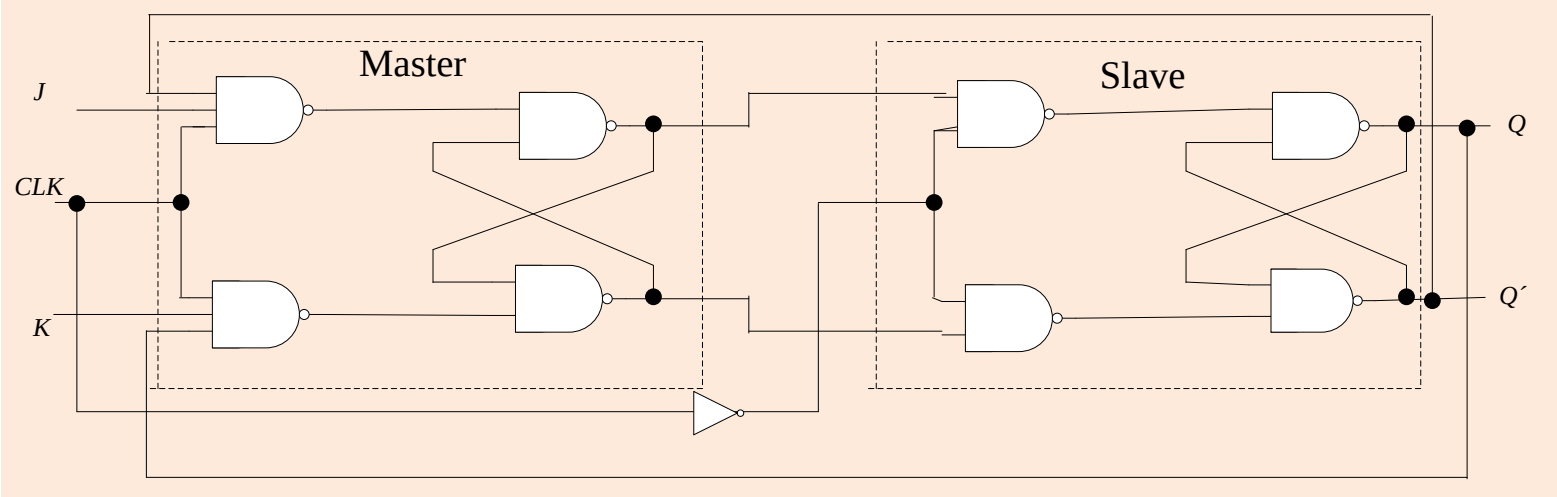


Positive edge triggered



$$Q_{n+1} = T.\overline{Q_n} + \overline{T}.Q_n$$

Master / Slave JK Flip Flops

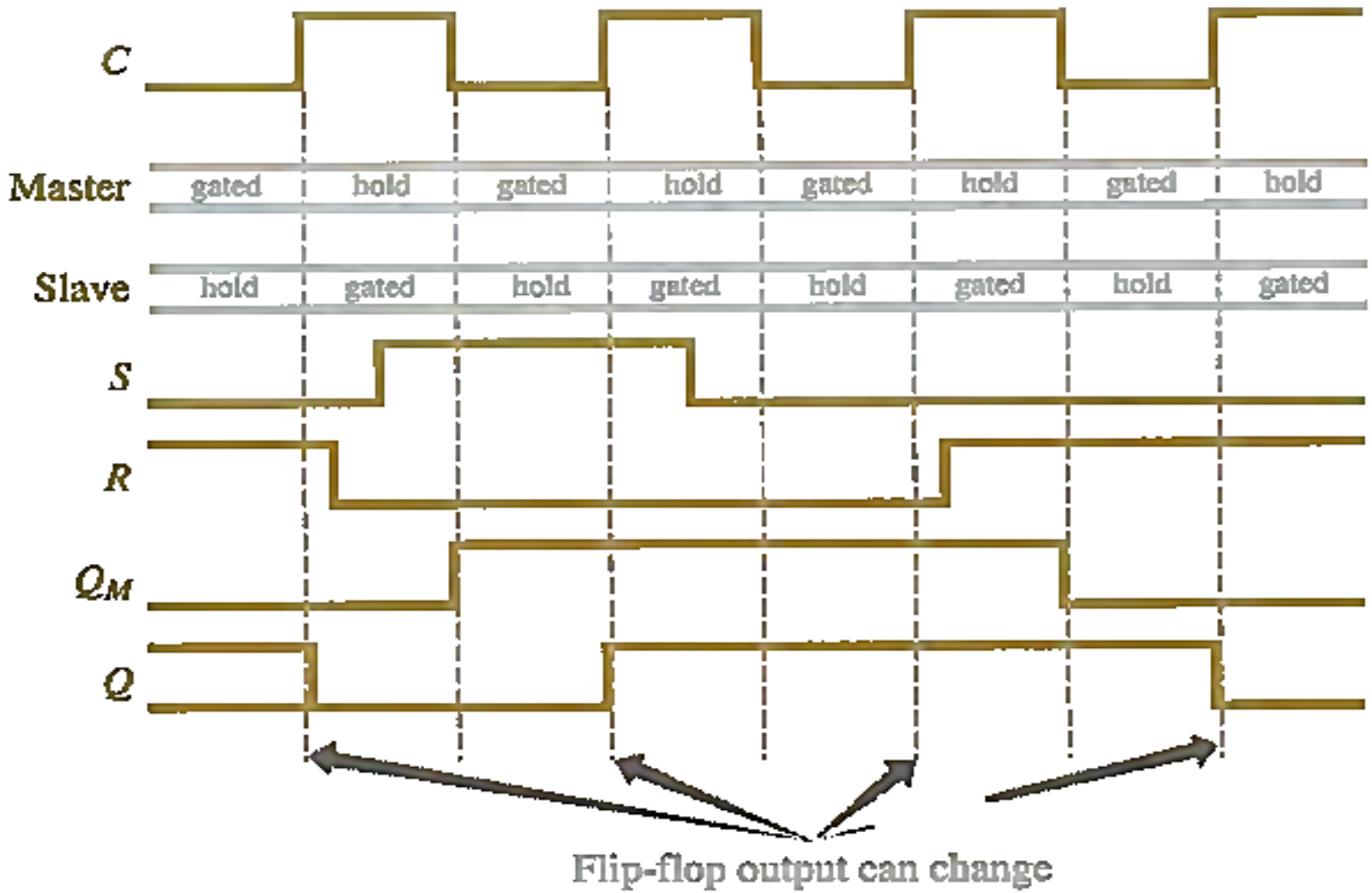


Clk { HIGH = Master enable; Slave isolate }

Clk { HIGH = Master isolate; Slave enable }

(Clk) High,

1.	$Q_S = 1,\ \overline{Q_S} = 0,$	J =1,	K = 0	Q_S , $\overline{Q_S}$ output (no-change)
2.	$Q_S = 0,\ \overline{Q_S} = 1,$	J =1,	K = 0	$Q_{S\ output} = 1$, $\overline{Q_S}$ output = 0)
3.	$Q_S = 1,\ \overline{Q_S} = 0,$	J =0,	K = 1	$Q_{S\ output} = 0$, $\overline{Q_S}$ output = 1)
4.	$Q_S = 0,\ \overline{Q_S} = 1,$	J =0,	K = 1	Q_S , $\overline{Q_S}$ output (no-change)
5.	$Q_S = X,\ \overline{Q_S} = X,$	J =0,	K = 0	Q_S , $\overline{Q_S}$ output (no-change)
6	$Q_S = 1,\ \overline{Q_S} = 0,$	J =1,	K = 1	$Q_{S\ output} = 0$, $\overline{Q_S}$ output = 1)
7.	$Q_S = 0,\ \overline{Q_S} = 1,$	J =1,	K = 1	$Q_{S\ output} = 1$, $\overline{Q_S}$ output = 0)


C
Master
gated
hold
gated
hold
gated
hold
gated
hold
Slave
hold
gated
hold
gated
hold
gated
hold
gated
S
R
Q_M
Q
Flip-flop output can change